CLAIM LISTING

No claims have been amended, added, or canceled. A Claim Listing is provided as a courtesy.

Claims 1-18 (Canceled).

19.   (Previously Presented) A device comprising:

micro-engines to receive a packet, determine if a task is available to process the packet, and to assign the task and a buffer to store the packet, said micro-engines comprising:

first circuitry to extract from a packet header comprising the packet a value representing a queue, and to signal a sequencer that a micro-engine task and cell buffer are to be assigned for the packet; and

second circuitry to extract an opcode for the packet header, determine a number of bytes in the packet header, to determine a number of bytes in the packet payload, and to determine a number of bytes available in the cell buffer.

20.   (Previously Presented) The device of claim 19, wherein the first circuitry comprises:

third circuitry to receive the packet and transmit a request that the micro-engine task be assigned to process the packet.

21.   (Previously Presented) The device of claim 20, wherein:

the sequencer is capable of receiving the request that the micro-engine task be assigned to process the packet, identifying if the micro-engine task is available to process the packet, and assigning the micro-engine task and the cell buffer to the packet.

22.   (Previously Presented) The device of claim 21, wherein the first circuitry also comprises:

a counter to count a number of packets received by the third circuitry and to transmit to the sequencer another value representing the number of packets received by the third circuitry; and

first-in-first-out (FIFO) circuitry to receive the value representing the queue and to transmit to the sequencer the value representing the queue.

23.   (Previously Presented) The device of claim 19, wherein the second circuitry comprises:

third circuitry to determine based upon the opcode a length of the packet header.